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EXAMINER	
ROSARIO-VASQUEZ, DENNIS	
ART UNIT	**PAPER NUMBER**
2621	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/855,011	RATCLIFFE, MARTIN J.	
	Examiner	Art Unit	
	Dennis Rosario-Vasquez	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amed, 10/15/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment was received on 10/15/2004 and entered. Claims 1-23 are pending.

Response to Arguments

2. Applicant's arguments, see amendment, pages 9-11, filed 10/15/2004, with respect to claims 21 and 22 have been fully considered and are persuasive. The rejection of claims 21 and 22 have been withdrawn.

3. Applicant's arguments, see amendment, pages 12-16, filed 10/15/2004, with respect to the rejection of claim 1 under Malinowski et al. (US Patent 5,574,572) and Shirota (US Patent 4,376,290) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Cahill, III et al. (US Patent 5,784,047 A).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims1,2,4,5,6,7,8,9,10,11,12,13,14,15,16,18,19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Cahill, III et al. (US Patent 5,784,047 A).

Regarding claims 1 and 15, Cahill, III et al. discloses an apparatus for variably scaling video picture signals comprising:

a) a first circuit and means (fig. 4,num. 108a-108c: VERTICAL SCALER) configured to generate one or more data signals vertically scaled to a first value (Outputs of fig. 4,numerals 108a-108c.) in response to said video picture signals (fig. 4,num. 104a-104c: "LB1" and num. 106a-106c: "LB0") and one or more first control signals(fig. 4, num. 118: DISPLAY CONTROL UNIT outputs a control signal to fig. 4,num. 108a-108c: VERTICAL SCALER.);

b) a second circuit and means (Fig. 4,num. 110a-110c: HORIZONTAL SCALER) configured to generate one or more output signals horizontally scaled to a second value (Output of figure 4,numerals 110a-110c.) in response (The outputs of fig. 4,numerals 108a-108c are inputted to figure 4,num. 110a-110c via numeral 109 to generate an output of figure 4,numerals 110a-110c in response to the signals of fig. 4,numerals 108a-108c.) to said one or more data signals (Outputs of fig. 4,numerals 108a-108c.) and (ii) said one or more first control signals (fig. 4, num. 118: DISPLAY CONTROL UNIT outputs a control signal to fig. 4,num. 108a-108c: VERTICAL SCALER and 110a-110c: HORIZONTAL SCALER.), wherein said first value (Outputs of fig. 4,numerals 108a-108c.) and said second value (Output of figure 4,numerals 110a-110c.) are independently selectable (Cahill states," With respect to vertical scaler 108 and horizontal scaler 110, scaling can be...independently programmable in both vertical and horizontal dimensions...(col. 9, lines 21-24)."); and

c) an address generator circuit and means (fig. 5,num. 116:VERTICAL AND HORIZONTAL DDA CONTROL & COUNTER UNIT generates an address in col. 9, lines 1-3.) configured to generate said one or more first control signals (fig. 4 or fig. 5, num. 118: DISPLAY CONTROL UNIT is a portion of figure 5,num. 116 and outputs a control signal or "VERTICAL WEIGHT" to fig. 4,num. 108a-108c: VERTICAL SCALER.), wherein said address generator (fig. 5,num. 116:VERTICAL AND HORIZONTAL DDA CONTROL & COUNTER UNIT generates an address in col. 9, lines 1-3.) comprises a finite state machine (fig. 6A, num.262:ADVANCE STATE MACHINE is contained in figure 5, num. 116: VERTICAL AND HORIZONTAL DDA CONTROL & COUNTER UNIT.) configured to allow multiple luma (Fig. 4,num. 102a:Y MEMORY is a luminance component.) and multiple chroma picture (Fig. 4,num. 102b: U MEMORY and 102c: V MEMORY are chrominance components.) requests to follow in sequence (LB1 and LB0 correspond to the luma and chroma signals that are fetched or requested in an "order" in col. 14, line 2 using figure 10, num. 107:PREFETCH BUFFER from col. 13, line 30 to col. 14, line 2.) .

Regarding claim 2, Cahill, III et al. discloses the apparatus according to claim 1 wherein said first circuit comprises:

(i) a luma circuit (Fig. 4,num. 102a: Y MEMORY) configured to generate a luma component(Fig. 4, num. 102a: Y MEMORY generates a luma or "Y" component.) of said data signals (Outputs of fig. 4,numerals 108a-108c includes a luma component 108 that originated from fig. 4, num. 102a: Y MEMORY.); and

(ii) a chroma circuit (Fig. 4, num. 102b: U MEMORY and 102c:V MEMORY have the same features as fig. 4, num. 102a: Y MEMORY, thus this limitation is addressed above using fig. 4, num. 102a: Y MEMORY and the respective components to numerals 102b and 102c.) configured to generate one or more chroma components of said data signals (Outputs of fig. 4,numerals 108a-108c.).

Regarding claim 4, Cahill, III et al. discloses the apparatus according to claim 1, wherein said apparatus is programmable (Cahill states," With respect to vertical scaler 108 and horizontal scaler 110, scaling can be... independently programmable in both vertical and horizontal dimensions...(col. 9, lines 21-24).") to scale said output signals (Output of figure 4,numerals 110a-110c.) to one or more display modes (fig. 3,num. 1000: VIDEO SYSTEM "supports various modes of operation...(col. 7, lines 46-48).").

Regarding claim 5, Cahill, III et al. discloses the apparatus according to claim 4 wherein said apparatus is configured to automatically reset a starting address (fig. 25, num. 1410: READ ADDRESS 720+724 has an address labeled "T12" that is reset at time "T3" of a READ STOBE 1408 of figure 25.) of a display line (A0 of figure 23 is a line of data P0, P2....) when an end (Fig. 25, num. 1404: W1 ACTIVE corresponds to the display line A0 and the address labeled "T12" that does not contain an end of display line because it contains only the first two data 0 and 1 of display line A0 while fig. 25,num 1406: W2 ACTIVE does contain the end "19" of a display line A0 in col. 24, lines 12-14.) of said display line (Fig. 23, label A0.) is not displayed (Thus, fig. 25,num. 1404: W1 ACTIVE does not display the end "19" of display line A0. On the other hand, fig. 25, num.1406: W2 ACTIVE does display the end of display line "19".).

Regarding claim 6, Cahill, III et al. discloses the apparatus according to claim 4, wherein said one or more output signals are scalable (Output of figure 4,numerals 110a-110c are scaled values.) to any value in a range of 0.25 times to 4.0 times (A range from 4:1 to 2:1 in col. 20, lines 53-55.) said video picture signals (fig. 4,num. 104a-104c: "LB1" and num. 106a-106c: "LB0").

Regarding claim 7, Cahill, III et al. discloses the apparatus according to claim 2, wherein said luma circuit comprises:

a) a first memory circuit (fig. 4,num. 107: VERT. PREFETCH BUFFER) configured to buffer a luma component (Fig. 4,num. 104:LB1 and num. 106:LB0 are luma components.) of said video picture signals (fig. 4,num. 104a-104c: "LB1" and num. 106a-106c: "LB0");

b) a first filter circuit (Fig. 3,num. 1022: VIDEO PROCESSOR filters in col. 7, line 51.) coupled to said first memory circuit (via figure 3 numerals 1009,1030 and figure 4, label "FROM DMA 1030" of figure 3 and num. 102.) and configured to generate said luma component (Fig. 4,num. 104:LB1 and num. 106:LB0 are luma components.) of said data signals (Outputs of fig. 4,numerals 108a-108c.); and

c) a second memory circuit (Fig. 4, num. 109: HORIZ. PREFETCH BUFFER 109.) coupled (via figure 3 numerals 1009,1030 and figure 4, label "FROM DMA 1030" of figure 3 and num. 102,107 and 108.) to said first filter circuit (Fig. 3,num. 1022: VIDEO PROCESSOR) and configured to buffer said luma component (Fig. 4,num. 104:LB1 and num. 106:LB0 are luma components.) of said data signals (Outputs of fig. 4,numerals 108a-108c.).

Claim 8 has the same features of claim 7 except for requiring a chroma circuit as disclosed by Cahill, III et al. in figure 4, numerals 102b and 102c with the same features of a luma circuit of claim 7 and a second filter circuit in figure 3,num. 1022 performs a filtering.

Regarding claim 9, Cahill, III et al. discloses the apparatus according to claim 1, wherein said generator circuit (fig. 5,num. 116:VERTICAL AND HORIZONTAL DDA CONTROL & COUNTER UNIT generates an address in col. 9, lines 1-3.) is configured to generate said control signals (fig. 4 or fig. 5, num. 118: DISPLAY CONTROL UNIT is a portion of figure 5,num. 116 and outputs a control signal or "VERTICAL WEIGHT" to fig. 4,num. 108a-108c: VERTICAL SCALER.) in response to one or more second control signals (Figure 5, label: "FROM RASTER CONTROL UNIT 1040") from a microcontroller circuit (fig. 3, num. 1040: RASTER CONTROL UNIT).

Regarding claim 10, Cahill, III et al. discloses the apparatus according to claim 9, wherein said apparatus comprises a single-chip MPEG-Z decoder (Fig. 3,num. 1022: VIDEO POROCESSOR includes a decoder in col. 7, line 51.).

Regarding claim 11, Cahill, III et al. discloses the apparatus according to claim 7, wherein said first filter circuit (Fig. 3,num. 1022: VIDEO PROCESSOR filters in col. 7, line 51.) further comprises one or more accumulator circuits (Fig. 5,num. 116: VERTICAL AND HORIZONTAL DDA CONTROL & COUNTER UNIT is an accumulator as mentioned in col. 8, line 57,58.) configured to define a number (fig. 5, num. 116 counts with a counter unit.) of said video picture signals (fig. 4,num. 104a-104c: "LB1" and num. 106a-106c: "LB0") be buffered in said first memory circuit (fig. 4,num. 107: VERT. PREFETCH BUFFER) in response to said one or more first control signals (fig. 4 or fig. 5, num. 118: DISPLAY CONTROL UNIT is a portion of figure 5,num. 116 and outputs a control signal to "VERT. PREFETCH BUFFER 107 via control signals "[M]UX SELECT" and "VERTICAL WEIGHT" to fig. 4,num. 108a-108c: VERTICAL SCALER.).

Claim 12 is has the same features as claim 11 except for requiring more of the same components. Thus, claim 12 was addressed in claims 8 and 11.

Regarding claim 13, Cahill, III et al. discloses the apparatus according to claim 1, wherein said second circuit (Fig. 4,num. 110a-110c: HORIZONTAL SCALER) controls an output rate (Fig. 4,num. 110a-110c: HORIZONTAL SCALER outputs a "processing rate" in col. 3, lines 13-16 regardless of slower components in col. 2, lines 57-67.) of said data signals (Outputs of fig. 4,numerals 108a-108c.) from said first circuit (fig. 4,num. 108a-108c: VERTICAL SCALER) in response to said first value (Outputs of fig. 4,numerals 108a-108c.) and said second value (Output of figure 4,numerals 110a-110c.).

Regarding claim 14, Cahill, III et al. discloses the apparatus according to claim 1, wherein said second circuit (Fig. 4,num. 110a-110c: HORIZONTAL SCALER) comprises (via signal "HORIZONTAL WEIGHT" of figure 5.) one or more accumulator circuits (Fig. 5,num. 116: VERTICAL AND HORIZONTAL DDA CONTROL & COUNTER UNIT is an accumulator as mentioned in col. 8, line 57,58.) configured to select one (Fig. 5,num. 116 is configured via a "[M]UX SELECT" signal to select data from a buffer 107 to be outputted from VERTICAL SCALER 108 of fig. 5.) or more of said data signals (Output of fig. 5,num. 108: VERTICAL SCALER or outputs of fig. 4,numerals 108a-108c.) in response to said one or more first control signals (fig. 4, num. 118: DISPLAY CONTROL UNIT outputs a control signal or signals "VERTICAL WEIGHT" and "[M]UX SELECT" to fig. 4,num. 108a-108c: VERTICAL SCALER and VERT. PREFETCH BUFFER 107, respectively.).

Claim 16 was addressed in claim 1.

Claim 18 was addressed in claim 13.

Claim 19 was addressed in claim 4.

Claim 20 was addressed in claim 5.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cahill, III et al. (US Patent 5,784,047 A) in view of Malinowski et al. (US Patent 5,574,572 A).

Regarding claim 3, Cahill, III et al. teaches the apparatus according to claim 1, wherein said second circuit (Fig. 4,num. 110a-110c: HORIZONTAL SCALER) is further configured to interpolate ("interpolation" in col. 3, line 14) said data signals (Outputs of fig. 4,numerals 108a-108c.).

Cahill, III et al. does not disclose decimation; however, Cahill, III et al. does suggest that "different scaling factor can be used" in col. 20, line 55. Thus, a scaling factor for decimating or shrinking or for interpolating or enlarging a data signal by scaling is suggested by Cahill, III et al..

However, Malinowski et al. does teach a use of an "Interpolator" in col. 3, line 40 to col. 4, line 52 and a "Decimating Filter" from col. 4, line 53 to col. 6, line 10 for scaling in col. 3, lines 25-39 as suggested by Cahill, III et al.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Cahill, III et al.'s teaching of interpolating with scaling with Malinowski et al.'s teaching of the decimating filter, because, Malinowski et al.'s decimating filter provides "a high quality scaled image (Malinowski et al. col. 2, lines 15-19)."

Claim 17 was addressed in claim 3.

8. Claims 21,22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cahill, III et al. (US Patent 5,784,047 A) in view of Ozcelik et al. (6,078,616 A).

Regarding claim 21, Cahill, III et al. does not teach the limitation of claim 21, but does suggest using a state machine in figure 6A,num. 262 ADVANCE STATE MACHINE that process chroma signals, U and V of figure 4. Note that the state machine is located within numeral 118 of figure 4.

However, Ozcelik et al. does teach claim 21 of an apparatus, wherein a finite state machine (fig. 6) comprises an idle after chroma state (fig. 6, num. 620 is a waiting state after a previous chroma state 614.) configured to move (via arrow direction of numerals 622,626 and 628) to a luma state (Fig. 6, num. 624).

Regarding claim 22 Ozcelik et al. does teach an apparatus wherein a finite state machine (fig. 6) comprises an idle after luma state (fig. 6, num. 620 is a waiting state after a previous luma state 606.) configured to move (via arrow direction of numerals 622,626 and 628) to a luma state (Fig. 6, num. 624).

Regarding claim 23 Ozcelik et al. does teach an apparatus, wherein a finite state Machine (fig. 6) provides (i) an idle after chroma state (fig. 6, num. 620 is a waiting state after a previous chroma state 614.) configured to move (via numerals 622,626,628,624,630) to a chroma state (fig. 6, num. 632 is a chroma state) in response to a first predetermined condition (output of 618 of fig. 6 is a previous process.) and (ii) an idle after luma state (fig. 6, num. 606 is a waiting state for luma data) configured to move to a luma state (fig. 6, num. 612) in response to a second predetermined condition (State 606 moves to 612 when 606 receives luma reference data.)

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Cahill, III et al.'s state machine with Ozcelik et al. state machine of figure 6, which is also shown as 502 coupled to a filter 504 as shown in fig. 5, because Ozcelik et al.'s state machine constructs a macroblock that effectively conceals an error in a data stream as mentioned in col. 4, lines 18-20 and col. 7, lines 57-61.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Snyder et al. (US Patent 5,363,119 A) is pertinent as teaching a method of scaling vertically fig. 4,num. 146 and horizontally using a state machine of figure 4, num. 154.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis Rosario-Vasquez whose telephone number is 703-305-5431. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Boudreau can be reached on 703-305-4706. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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